REMARKS/ARGUMENTS

This paper is responsive to the Non-Final Office Action dated December 15, 2004, having a shortened statutory period expiring on March 15, 2005, wherein:

Claims 1, 3-12, 14, 15, 17-20, 22-25, and 27-29 were pending in the application;

Claims 5, 19, 24, and 29 were objected to; and

Claims 1, 3, 4, 6-12, 14, 15, 17, 18, 20, 22, 23, 25, 27, and 28 were rejected.

No claims have been amended, added, or canceled herein. Consequently, claims 1, 3-12, 14, 15, 17-20, 22-25, and 27-29 remain currently pending in the present application.

Formal Matters

On the cover page, as well as page 10 of the present Office Action, it is indicated that Applicants' claims 5, 19, 24, and 29 are objected to as being dependent upon a rejected base claim, but would otherwise be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Applicants believe that this objection was made mistakenly. Elsewhere in the present Office Action, it is indicated that, "The examiner maintains that claims 5, 19, 24 and 29 are allowable, and is unclear as to whether applicant's amendment to make them independent claims indicates a willingness to cancel other claims to make [the] application allowable, possibly with a continuation to re-prosecute cancelled claims."

In fact, Applicants did not, and do not intend to cancel any claims, either previously or at this juncture. In accordance with the prior indication of allowable subject matter (see Final Office Dated March 30, 2004) Applicants previously amended claims 5, 19, 24, and 29 in independent form. Consequently, Applicants respectfully submit that the indicated claims (5, 19, 24, and 29) are allowable, notwithstanding Applicants having not canceled remaining claims 1, 3, 4, 6-12, 14, 15, 17, 18, 20, 22, 23, 25, 27, and 28. Applicants therefore respectfully request an indication of allowability thereof, as well as claims depending on (now independent) claims 5, 19, 24 and 29.

Applicants further wish to express their appreciation for the Examiner's indication of allowable subject matter.

Examiner's Response to Arguments

The present Office Action responds to the arguments of Applicants' Response to Non-Final Office Action filed January 22, 2004. Applicants appreciate the consideration reflected therein, but respectfully traverse the position taken therein as follows.

In paragraph 4 of the present Office Action, an attempt has been made to clarify an interpretation of the term "deconstructing" to be encompassed by the term "filter" or "filtering" as taught by United States Patent No. 5,951,651, issued to Lakshman et al. (hereinafter "***Lakshman***"). While Applicants maintain that the filtering of information would not have been considered to be a form of deconstruction (and should not be so considered), the terms "filtering" and "deconstruction" have been considered equivalent for the sake of argument within this response.

In the present Office Action (see paragraph 6, pages 3 and 4), it is stated that,

> ...the first step of filtering based upon header data is to determine the header data from a previously constructed packet, and thus the deconstruction to get the data is inherent (col. 4, line 48 – col. 5, line 5). Furthermore, Lakshman teaches that element 250a receives the incoming packet and stores the parameter in a register (col. 6, lines 10-15, hence explicitly teaching this step.

Applicants have interpreted this portion of the present Office Action as indicating that elements 250, as taught by ***Lakshman***, teach filtering of a packet, and therefore inherently teach "deconstructing" as claimed. Applicants respectfully disagree.

Lakshman teaches that processing elements 250a...250n are used to receive an incoming packet, store a parameter in register 276, perform a comparison to ascertain the correct window partition to apply to the received packet, and to determine and output a corresponding bitmap vector containing potential filter rules (see, e.g., ***Lakshman***, Column 6, Lines 12-24). ***Lakshman*** further teaches however that,

> ...the binary searching method is performed whereby parameter information from the window array is input to the register 279 and comparator 280 performs a comparison to ascertain the correct window partition w_i to apply to the received packet. After the correct window partition is found, its corresponding bitmap vector containing potential filter rules is output of register 279 along line 290.

> Referring back to FIG. 8(a), once the corresponding bitmap vectors are determined from each processing element 250a, ..., 250n, for each dimension, the vectors are input to logic circuitry 295 for performing the intersection, i.e., logical AND operation. From the resultant bitmap vector, the CPU will apply the rule of highest priority, and performs the action dictated by the rule upon the received packet stored in the pipeline register 225. Thus, the packet may be dropped or forwarded to another destination on output line 215. (***Lakshman***, Column 6, Lines 17-33, emphasis supplied)

Thus, ***Lakshman*** explicitly teaches that "filtering" is performed by a central processor (CPU) once a bitmap vector has been determined using processing elements 250a...250n. As none of processing elements 250 are taught by ***Lakshman*** as being used for "filtering" Applicants submit that they cannot be construed as being used to perform "deconstructing" according to ***Lakshman***'s teaching, even accepting *arguendo* that "filtering" is a form of "deconstruction," as proposed in the Office Action. Consequently, it is respectfully submitted that ***Lakshman***, as interpreted in the Office Action, fails to teach "a second peripheral processor" (emphasis supplied) used to deconstruct a packet header to form header data as claimed (Applicants' claim 1).

Claim Rejection under 35 U.S.C. § 103

In the present Office Action, claims 1, 3, 4, 6, 7, 9-12, 14, 15, 17, 18, 20, 22, 23, 25, 27, and 28 were rejected under 35 U.S.C. 103(a) as being unpatentable over ***Lakshman*** in view of U.S. Patent No. 6,101,551, issued to Kanoh (hereinafter "***Kanoh***"). While not conceding that the Examiner's cited reference(s) qualify as prior art, but instead to expedite prosecution, Applicants have elected to respectfully disagree and traverse the rejection as follows. Applicants reserve the right, for example, in a continuing application, to establish that one or more of the Examiner's cited references do not qualify as prior art as to an invention embodiment previously, currently, or subsequently claimed.

In the present Office Action, it is stated with regard to Applicants' claim 1 that, while ***Lakshman*** does not expressly disclose that there are multiple processors with differing functionality,

> Lakshman teaches that there is an array of differing functional elements (Fig. 8a, #250) and that each one has processors for different tasks (Fig. 8b, #250) which

> may be formed as an ASIC or FPGA (col. 5, line 65 – col. 6, line 10). Kanoh teaches a method (abstract) of spreading out such functionality over a variety of processors (col. 1, line 1 – col. 4, line 5), wherein different functions are on different chips (Fig. 1, #1) within a circuit board.

Further, Official Notice under MPEP §2144.03) is taken in the Office Action with regard to the statement that "different steps on different processors" in a computer networking environment was well known in the art at the time Applicants' invention was made and that, "one of ordinary skill in the art would have used Kanoh to better determine a hardware embodiment for Lakshman and to perform a high-speed receiving processing (col. 1, lines 55-65). Applicants respectfully disagree.

Applicants submit that the present Office Action has failed to state a *prima facie* case of obviousness under 35 U.S.C. §103. The Office Action fails to state with sufficient specificity, as required by 37 C.F.R. §1.104(c)(2), where within ***Kanoh***'s disclosure, "spreading out such functionality over a variety of processors" is taught, shown, or suggested.

Moreover, Applicants submit that the teachings of ***Kanoh*** and ***Lakshman*** are contrary to one another. Consequently, one of ordinary skill in the relevant art would not have been motivated to combine their teachings as suggested in the Examiner's rejection.

Kanoh teaches a multi-processor system for supporting multicasting communication and inter-multiprocessor communication including a plurality of processors (1 and 1a) wherein,

> A packet is held in a FIFO memory through a network. The packet includes a header and data. The header includes fields of a packet type, a data length, and a designation for a processor. The packet type field defines whether its packet is either a single-cast packet or a multi-cast packet and a designation method for a destination address. There are several methods for the destination address: first, a method using a message buffer in a memory, secondly, a method using a value of an address register previously set, and thirdly, a method designating as a destination address. The (original) entity of the address register may be reserved in the memory. In this case, different message buffers for every task identifier may also be reserved in the memory. (***Kanoh***, Abstract, see also ***Kanoh***, Column 2, Lines 46-48)

Kanoh further teaches that, "In the multicasting communication, the data is transferred to the specified processor that is previously designated, unlike a broadcast to

transfer the data to all of the processors." (***Kanoh***, Column 1, Lines 32-34, emphasis supplied) According to the teaching of ***Lakshman*** by contrast, "The incoming packet is input to a pipeline register 225 for temporary storage and is also input to each processing element indicated as elements 250a, ..., 250n corresponding to each dimension k=1 to k=n." (Lakshman, Column 6, Lines 7-10, emphasis supplied). Applicants submit that one of ordinary skill in the relevant art would not have been motivated to use a system for selectively transmitting data to a designated processor of a group or set (multicasting) as taught by ***Kanoh***, in conjunction with a system for transmitting an incoming packet to each of a number of processing elements (effectively broadcasting) as taught by ***Lakshman***.

In addition to the those arguments previously made by Applicants which are maintained and the indicated allowability of claims 5, 19, 24, and 29, Applicant submit that for at least the foregoing reasons, claims 1 and 6 are allowable over the Examiner's cited references. Applicants further submit that all remaining claims, depending directly or indirectly from Applicants' claims 1 or 6, are allowable for at least the reasons stated for the allowability of the corresponding claim(s) from which they depend.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5084.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, COMMISSIONER FOR PATENTS, P. O. Box 1450, Alexandria, VA 22313-1450, on February 10, 2005.

Attorney for Applicant(s) — Date of Signature: 2/10/05

Respectfully submitted,

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